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EXAMINER	
PAN, DANIEL H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/648,293	FRANCIS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1.

2. Claims 1-62 are presented for examination.

1. Applicant's arguments with respect to claim claims 1-17,21-38, 42-58,62 rejected under 35 U.S.C. 102(b) as being anticipated by Ohshima (5,598,544) have been considered but are moot in view of the new ground(s) of rejection. In response to applicant's newly amended feature of the triggering of memory abort , and new reference ; Watt (5,802,598), has been introduced to show the memory abort. Also, claims 18-20, 39-41, 59-61 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima (5,598,544) in view Watt (5,802,598) as applied to claims 1, 22, 43 , and further in view of Komatsu (6,324,686). Reasons of obvious ness have been included in this action below.

2. In response to newly amended claim 22-42, the rejection of "101" to claim 22-42 has been canceled. Claim 22 now recites clearly the "circuitry". However, the rejection of "101" claims 43-62 has been maintained.

3. Response to applicant's remarks will be included in this action in order to clarify the "101" and teaching of art of record.

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 43-62 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The evidence shows that applicant's embodiment can be done in mixed hardware and software, and it can be also done in pure software (see page 15, lines 6-13).

5. As to claims 24-42, all dependent claims include the limitation of logic operable to detect, concatenate, restore, and divert. However, logic is an abstract idea. Therefore, non-statutory.

6. As to newly amended claim 43, the evidence shows that applicant's embodiment can be done in mixed hardware and software, and it can be also done in pure software (see page 15, lines 6-13). Furthermore, no specific elements of the program product have been reflected into the claim body to support the program product in the preamble. Therefore, no substantial practical application can be found for program product. Hence, no useful , tangible, and concrete results can be determined. Although claim 43 recites the instruction code embodied in a medium readable by data processing apparatus, it does not restricted into hardware. Instead, it included both the hardware [hardware] and pure software (see page 15, lines 6-13). Although the concatenated code encoded in the storage medium which when executed by the apparatus, controls the data processing apparatus, it is intended use, no useful, tangible, and concrete final result can be found for the concatenation of the instruction data. The final result of controlling the data processing apparatus is unclear. Therefore, no substantial practical application can be determined. Although claim recites storage medium and data processor, they are directed to a general arrangement of the elements. Since applicant taught "pure software", the computer program product is not restricted to hardware or hardware and software combination.

7. As to applicant's remark that applicant is not reciting program per se (see page 1 of the remark), examiner would like to point out that applicant also taught his invention

is implemented in "pure software" in addition to the hardware (see page 15, lines 6-13). Therefore it raised a doubt as what applicant intended to claim.

8. The dependent claims add no substantial practical application to the independent claim 43. See also Paragraphs 3-6 for similar features.

9. The examiner has reason to believe that the claim is not for a practical application that produces a useful result, the claim should be rejected, thus requiring the applicant to distinguish the claim from the three § 101 judicial exceptions to patentable subject matter by specifically reciting in the claim the practical application. In such cases, statements in the specification describing a practical application may not be sufficient to satisfy the requirements for section 101 with respect to the claimed invention. Likewise, a claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of a § 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected.

10. The claim does not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. Hence, no useful , concrete , and tangible results can be determined. Specifically, applicant is clearly not limiting his embodiment in hardware (e.g. purely implemented in the form of software , page 15, lines 6-13).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17,21-38, 42-58,62 rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima (5,598,544) in view of Watt (5,802,598).

3. As to claim 1, 22,43, 43, Ohshima disclosed at least :

a) detecting an attempt to execute a variable length instruction spanning two discrete memory address regions (see fig.7A) , the two discrete memory address regions (see the basic segment 1 and basic segment 2) being a current memory address region and a following memory address region (see also fig. 515 to see how pointer P was used to address leading end of segment in the memory 403);

b) concatenating instruction data from an end portion of the current memory address region and a start portion of following memory address region into a fix-up memory address region of said memory (see the read out position by pointer P in col.2, lines 38-50) to form concatenated instruction data containing said variable length instruction (instruction code unit length, see also the concatenation of instruction fields in fig.1 and fig.5 , see also fig.7B, Ohshima's warp-around feature was a concatenation);

c) diverting program execution flow to execute the current variable length instruction from within the concatenated instruction data in the fix-up memory address region (see the execution unit 13 in fig.4 and fig.8C, for fixed up address see rearranged P pointer); and

(d) restoring program execution flow to execute instructions (execution not explicitly shown, but see execution unit [13] in 4) following the variable length instruction from within following memory address region (see next instruction segment in the memory region [404] in fig.5).

4. Ohshima did not specifically teach the triggering of the memory abort as claimed. However, Watt taught bits of variable size subsection from the address space were set to cause a memory abort generator to generate a memory abort signal. (col.4, lines 45-53). It would have been obvious to one of ordinary skill in the art to use Watt in Ohshima for triggering the memory abort as claimed because the sue of Watt could provide Ohshima the ability to preserve a particular memory range, thereby avoiding the data loss due to improper memory address space access. And, it could be implemented by predefining the abort signal of Watt in Ohshima with modified system variables (e.g. the specific type of abort signal for read and write), so that memory abort of Watt could be recognized by Ohshima, and because Ohshima also taught that execute a variable length instruction spanning two discrete memory address regions (see fig.7A) , the two discrete memory address regions , see the basic segment 1 and basic segment 2, see also fig. 515 to see how pointer P was used to

address leading end of segment in the memory 403), which was a suggestion of the need for including an indication or a signal for memory abort due to the access to wrong memory address regions likely to occur, and for the above reasons , provided a motivation.

11. As to the remarks regarding the fix-up memory address region and Ohshima's code bus, see rearranged P pointer as a fixed up address in fig.4 and fig.8C). The address pointer defined the address region. See also fig.2a,b for fix up memory region.

5. As applicant's remark that decoding always takes place from Ohshima's instruction code bus, as result there is no need for divert program execution, examiner would like to point out that the fact that decoding always takes place, it does not necessarily mean that execution can be diverted. Execution can be diverted even after decoding.

6. The two basic segments were at discrete addresses because the corresponding expanded segment had a variable length (see 7, lines 1-5). Therefore, the second basic segment could start at any position. Also the first basic segment was shown to have a random position in fig.7A. See also variable instruction length in the background in col.1, lines 14-27.

12. Ohshima disclosed variable length instructions (see fig.7A) stored within a plurality of discrete memory address regions (see basic segment 1 and basic segment 2, see also figs.4 and 6A, code blocks);

13. Examiner would like to point out that two discrete memory address regions are not necessarily separate or non-continuous (see basic segment 1 and basic segment 2 in fig.7A).

14. Ohshima taught diverting the execution flow to execute current variable length instruction (see execution unit for execution) from the concatenated instruction data in the fix-up memory region (see the variable length instruction segments in fig.2a,b).

7. As to applicant's remark that one of ordinary skill in the art would to equate instruction code bus to the fix-up memory address region -- bus and memory are two different things, examiner would like to point out that one of ordinary skill in the art should be able to recognize an instruction code defines the memory address space. For example, a load command code is generally represented as :

8. L R1, Mem.

9. That is Loading from a Mem memory location to register R1. The Mem is an address space, or the memory address region. In other words, without an instruction code defining the memory address region, the memory address region would have no meaning.

As to applicant's remark regarding no teaching of Ohshima which corresponds to

"concatenating instruction data from an end portion of said current memory address region and a start portion of said following memory address region into a fix-up memory address region of said memory," as recited by the independent claims, examiner holds that Ohshima taught concatenating instruction data from an end portion of a current memory address region and a start portion of a following memory address region into a fix-up memory address region of the memory (see the read out position by pointer P in col.2, lines 38-50, see instruction code unit length, see also the concatenation of instruction fields in fig.1 and fig.5 , see also fig.7B, Ohshima's warp-around feature was a concatenation)

10. As to claim 22, claim 2 is directed to the same scope as claim 1 in apparatus .

11. As to claim 43, claim is directed the same scope as claim 1 in program product format. The examiner holds that this program product is not given a patentable weight because no specific recitation in the body of the claim reflects the specific elements of the program product.

12. As to claim 2,23, Ohshima also included hardware control (see fig.11).

13. As to claim 3, 24, Ohshima also included software control (see micro ROM control in col.7, lines 40-42, see also PLA).

14. As to claims 4,25,45, 46, the structural relation between the memory and the instruction buffer has been reflected into the claim, therefore, Ohshima also included instruction buffer (see the instruction buffer in fig.6A, this instruction buffer include the instruction storage 403, see also readout buffer at the output of storage 3 in fig.7B)

15. As to claims 5,26,47, see instruction fetched from the memory [430] to an instruction buffer [instruction register] before being executed in fig.4).

16. As to claims 6,27, Ohshima also included sequential addresses (see the entry 404 404' 404").

17. As to claims 7,8,27,28,29, 48,49, Ohshima also marked the valid instruction (see the marking for indicate whether to simultaneously decode the segments in col.7, lines 54-65, col.10, lines 28-48).

18. As to claims 9, 30, 50, Ohshima also disclosed a program counter (see program counter in col.2, lines 41-43).

19. As to claims 10,31,51, see how the program counter P readjusted to the leading position in col.8, lines 10-53).

20. As to claims 11,12, 13, 14,32,33,34, 35,52,53,54, 55, for the flag for single variable instruction length , see the instruction unit length in col.2, lines 48-50, see the L in the position identifying circuit in col.15, lines 56-58, col.16, lines 1-9).

21. As to claims 16,17, 36,37,38, 56, 57, 58, Ohshima also to point to the next instruction following the current instruction (see how the use of pointer 7 to point each of the 7 fields in a given entry 4 in col.8, lines 10-23, for calculation , see calculation of address in col., lines 40-54 for background) . AS to the diversion, it is read as pointer action (see the pointer P of Ohshima).

22. As to claims 21, 42, 62, see instruction storage 403 in fig.4.

23. As to claims 18-20,39-41,59-61, limitations of parent claims 1,22,43 have been discussed above, therefore, will not be repeated herein. Neither Ohshima nor Watt specifically taught the java byte code as claimed. However, Komatsu disclosed a java byte code of variable length (see col.1, lines 56-60). It would have been obvious to use the java by code as claimed because the use of Komatsu could provide Ohshima the ability to process his variable length instruction in a different type of language , such as the by codes, or like, and therefore, increasing the control adaptability of Ohshima, and because Ohshima already taught the rearrangement of his variable length instruction fields , one of ordinary skill in the art should be able to recognize the applicability of petitionable program codes, such as the byte codes , which was already taught by Komatsu to be used in a variable length instruction, into Ohshima in order to enhance the system compatibilities, and for doing so, provide a motivation.

24. As to the further instruction set in claim 19 , Komatsu also included a further instruction set (see C++ programming in col.1, lines 30-35).

25. As to the branch in claim 20, Ohshima already taught branch (see jump in col.7, lines 54-65).

26. Ohshima (5,598,544) and Komatsu (6,324,686) were cited on record. Therefore, they are not included in this action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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12. 21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP